WHAT IS CLAIMED IS:

1. A method of adjusting an analog actual signal to a digital desired signal using a circuit that includes a comparator having two input ports and one output port and an integrated digital-to-analog converter, said method comprising:

feeding the analog actual signal to one input port of the comparator;

feeding an analog output signal of the digital-to-analog converter to the other input port of the comparator;

feeding the digital desired signal as a digital input signal to the digital-to-analog converter;

adapting the digital input signal fed to the digital-to-analog converter as a function of an output signal of the comparator, in a definable number of iterative steps, between definable lower and upper thresholds according to a balancing process, the digital input signal in each case fed to the digital-to-analog converter corresponding to the digital desired signal to which the analog actual signal is converted.

2. The method according to Claim 1, wherein the analog actual signal corresponds to a burst comprising a definable number of pulses.

3. The method according to Claim 2, wherein:

a preselectable reference pulse from the burst is fed to the comparator; and

based on the reference pulse, in the comparator, a signal value is processed which corresponds to the pulse center.

4. The method according to Claim 1, wherein the number of the definable iterative steps corresponds to a bit length by which the digital desired signal is expressed.

5. The method according to Claim 1, wherein the digital desired signal is verified by a procedure in which:

for a first additional iterative step, a definable signal value is subtracted from the analog actual signal forming a diminished actual signal;

the diminished actual signal is then fed to an input port of the comparator;

the output signal of the comparator is checked to determine whether it falls below the analog output signal of the digital-to-analog converter, which is present at the other input port of the comparator and is generated from the digital desired signal to be verified; and

for a second additional iterative step, a correspondingly definable signal value is added to the analog actual signal forming an augmented actual signal;

the augmented actual signal is then fed to an input port of the comparator;

the output signal of the comparator is checked to determine whether it exceeds the analog output signal of the digital-to-analog converter, which is present at the other input port of the comparator and is generated from the digital desired signal to be verified; and

the digital desired signal is assumed to be correct when a result of the testing steps in the first and second additional iterative steps was affirmative.

6. A circuit for adjusting an analog actual signal to a desired digital signal, said circuit comprising:

a comparator having two analog input ports and one analog output port; and

a digital-to-analog converter having one digital input port and one analog output port; wherein,

the analog output port of the digital-to-analog converter is connected with one input port of the comparator;

the analog actual signal is fed to the other input port of the comparator; and

the analog output port of the comparator is connected with an electronic component for generating the desired digital signal which is fed to the digital input port of the digital-to-analog converter.